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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,902	11/13/2003	Naoki Mitsuishi	HITA.0453	6107

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EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,902	MITSUISHI, NAOKI	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 8-15 are objected to because of the following informalities: references in the claims to "the first through third buses" should be "the first, second, and third buses". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 is rejected because it is not clear what is meant by "the device requests a bus access right of the one bus at a predetermined timing for read operations of the other bus granted a bus access right."

Claim 4 is rejected because it depends on claim 3.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1,2,5, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Bell et al., U.S. Pat. No. 6,021,451.

As per claim 1, Bell shows a data transfer device (400) which is connected to first (401) and second (402) buses and transfers data between these buses, wherein the device can independently request a bus access right and output an address to the first and second buses, and the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing in response to one data transfer start request (col.7, line 50 – col.20 which describe the operation of the bridge 400 and how it operates to transfer transactions between the buses, wherein the bridge operates to read data from one bus and write the data to the other bus along with arbitrating for access to the buses to do the reading and writing). Bell shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Bell also shows that the device requests a bus access right of the one bus and requests a bus access right of the other bus at different timings (col.8, wherein arbitration units 411 and 451 are separate and they request bus access rights at different times). Bell shows all of the elements recited in claim 2.

As per claim 5, Bell shows a semiconductor integrated circuit comprising: a first bus (401); a second bus (402); a data transfer device (400) to transfer data between the first and second buses; a central processing unit (fig.2,(202)) connected to the first bus; and program storage memory (221) which stores a control program for the central processing unit and is connected to the first bus, wherein the data transfer device can independently request a bus access right and output an address to the first and second buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing

at a different timing in response to one data transfer start request, and wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second bus by means of the data transfer device (col.7, line 50 – col.20 which describe the operation of the bridge 400 and how it operates to transfer transactions between the buses, wherein the bridge operates to read data from one bus and write the data to the other bus along with arbitrating for access to the buses to do the reading and writing). Bell shows all of the elements recited in claim 5.

As per claim 6, Bell shows a semiconductor integrated circuit comprising: a first bus (401); a second bus (402); a data transfer device (400) to transfer data between the first and second buses; a central processing unit (202) connected to the first bus; and a bus control means for the first and second buses (in the bridge, there are arbitration blocks 411 and 451 along with the transaction arbitration unit 418), wherein the data transfer device can independently request a bus access right and output an address to the first and second buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first and second buses independently (col.7, line 50 – col.20 which describe the operation of the bridge 400 and how it operates to transfer transactions between the buses, wherein the bridge operates to read data from one bus and write the data to the other bus along with arbitrating for access to the buses to do the reading and writing). Bell shows all of the elements recited in claim 6.

6. Claims 7-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig, U.S. Pat. No. 6,567,880 B1.

As per claim 7, Olarig shows a semiconductor integrated circuit comprising: a first bus (103); a second bus (109); a third bus (107); a central processing unit (102) connected to the first bus; program storage memory (106) which stores a control program for the central processing unit and is connected to the first bus (via the bridge); and a data transfer device (104) capable of data transfer between the second and third buses, wherein the data transfer device can independently request a bus access right and output an address to the second and third buses, the device requests a bus access right of one bus for reading and requests a bus access right of the other bus for writing at a different timing in response to one data transfer start request, and wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second or third bus by means of the data transfer device (at least cols.12-13, wherein the operation of the bridge/core logic circuit 104 is explained. The PCI/PCI bridge 220 operates such that bus 109 and 107 can exchange data, and the various arbiters and control elements allow for the reading of data from one bus and writing the data to another bus, this is the function of any bus bridge). Olarig shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 7 applies. Olarig also shows a bus control means for the first through third buses, wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first through third buses independently (see at least fig.2, wherein the various arbiters and control elements perform the bus arbitration for bus access rights). Olarig shows all of the elements recited in claim 8.

As for claim 9, the argument for claim 8 applies. Olarig also shows that the central processing unit can access the second or third bus from the first bus via the bus control means (at least in cols. 12-13). Olarig shows all of the elements recited in claim 9.

As per claim 10, Olarig shows a microcomputer comprising: a first bus (103); a second bus (109); a third bus (107); a central processing unit (102) connected to the first bus; program storage memory (106) which stores a control program for the central processing unit and is connected to the first bus (via the core logic); and a data transfer device (104) capable of data transfer between any two of the first through third buses, wherein the data transfer device can independently request a bus access right and output an address to the first through third buses, and the device requests a bus access right of one bus for reading and requests a bus access right of the other buses for writing at a different timing in response to one data transfer start request (at least cols.12-13, wherein the operation of the bridge/core logic circuit 104 is explained. The PCI/PCI bridge 220 operates such that bus 109 and 107 can exchange data, and the various arbiters and control elements allow for the reading of data from one bus and writing the data to another bus, this is the function of any bus bridge). Olarig shows all of the elements recited in claim 10.

As for claim 11, the argument for claim 10 applies. Olarig also shows that the central processing unit is capable of bus access using the first bus in parallel with bus access using the second or third bus by means of the data transfer device (cols. 12-13). Olarig shows all of the elements recited in claim 11.

As for claim 12, the argument for claim 11 applies. Olarig also shows a bus control means for the first through third buses, wherein the bus control means is capable of arbitration of bus access right requests and bus control for the first through third buses independently (see at least fig.2, wherein the various arbiters and control elements perform the bus arbitration for bus access rights). Olarig shows all of the elements recited in claim 12.

As for claim 13, the argument for claim 12 applies. Olarig also shows that the central processing unit can access the second or third bus from the first bus via the bus control means (at least in cols. 12-13). Olarig shows all of the elements recited in claim 13.

As for claim 14, the argument for claim 10 applies. Olarig also shows that the data transfer device has a plurality of data transfer channels and a control register to specify data transfer channel operations, and wherein the control register has a transfer request generation source specification area for defining correspondence between a data transfer channel to receive a transfer request and a transfer request generation source; a source bus specification area for defining correspondence between a data transfer channel and a transfer source bus; and a destination bus specification area for defining correspondence between a data transfer channel and a transfer destination bus (cols. 12-13 and figs.2,2A,3,3A, where the various control elements and registers are used to transfer data between the various buses and the channels are 209,211, and the line coupling bus 109 to PCI/PCI bridge 220). Olarig shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 14 applies. Olarig also shows that a central processing unit can access the control register (cols. 12-13). Olarig shows all of the elements recited in claim 15.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references show other bus bridges.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
28 October 2005